

REMARKS

Claims 1-24 are pending in this application. By this Amendment, claims 1 and 8-15 are amended. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attachment is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

The Office Action objects to the claims because they include reference characters that are not enclosed within parenthesis. The above amendments to claims 1 and 8-15 provides parenthesis around various reference characters such as VIN, VCK and WL. Withdrawal of the objection of the claims is respectfully requested.

Applicants gratefully acknowledge the Office Action's indication that claims 13-15 are allowed and that claims 6-9, 21 and 23-24 are allowable over the prior art.

The Office Action rejects claims 1-5, 10-12, 16-20 and 22 under 35 U.S.C. §102(e) by U.S. Patent 6,472,917 to Yamauchi et al. (hereafter Yamauchi). The rejections are respectfully traversed.

Independent claim 1 recites a first long-distance wiring connected to a driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring. Independent claim 1 also recites a node arranged in the vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-

increasing circuit.

For example, as discussed in the present application, a second long-distance wiring 106 and a speed-increasing circuit 107 may be arranged in parallel to the driver circuit 100 and a first long-distance wiring 104. The two parallel lines may be connected at the input terminal of the driver circuit 100 and at the node 105 in the vicinity of an input terminal of the gate circuit 103. As discussed in the present specification, a signal change may be accelerated not only from one end of the driver circuit 100 but also from the other end by using the second long-distance wiring 106 and a speed-increasing circuit 107, thereby enabling to significantly reduce the wiring delay time and increase the critical path speed as well as to improve the operation speed of the semiconductor integrated circuit device. See page 4, lines 14-28 and page 7, line 7-page 8, line 18 of the present specification.

The Office Action references Yamauchi's Figures 3 and 6 as showing the claimed features. More specifically, the Office Action asserts Yamauchi's clock CK corresponds to the claimed input signal (VIN). However, Yamauchi's clock CK is input to the precharge circuits (100, 600) and speed-increasing circuits (800, 1200 and 1300). That is, in Yamauchi, the operations of the circuits 100, 600, 800, 1200 and 1300 are controlled by a clock CK. This clearly differs from embodiments in the present specification in which operation of the circuits are controlled without using this type of clock signal. The use of the claimed input signal (VIN) is completely different from Yamauchi's clock CK.

Applicants are unable to determine the Office Action's interpretation of the

claimed first long-distance wiring and the claimed second long-distance wiring. For example, if the wiring between Yamauchi's lines 400 (Figure 6) is assumed as the first long-distance wiring, then Yamauchi does not include the claimed second long-distance wiring. If the clock CK line is assumed to be the second long-distance wiring, then Yamauchi's structure clearly differs from the present application (and as set forth in claim 1). In Yamauchi's Figure 6, the clock CK is connected to all of the speed increasing circuits 1200 and 1300. Additionally, in Yamauchi's Figure 3, the speed increasing circuit 800 starts to operate in response to detection of a variation of signal 803 at the input of the gate circuit and increases the speed of the signal variation.

These features of Yamauchi differ from the present application in which the speed increasing circuit 107 is driven with the second long-distance wiring without waiting for a signal via a plurality of gate circuits 103. Because of this, the rate of speed increasing (in the present application) is much higher than in Yamauchi.

Accordingly, Yamauchi does not teach or suggest the claimed first long-distance wiring, second long-distance wiring and the node arranged in the vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected to the second long-distance wiring and a speed-increasing circuit. Accordingly, independent claim 1 defines patentable subject matter. Each of independent claims 10-12 and 16 define patentable subject matter for at least similar reasons as claim 1.

Each of claims 2-5, 17-20 and 22 depend from one of the independent

claims, and therefore also define patentable subject matter. In addition, the dependent claims also recite features which further and independently distinguish over the applied prior art.

For at least the reasons set forth above, it is respectfully submitted that each of claims 1-24 define patentable subject matter. Withdrawal of the outstanding rejections are respectfully requested.

The Office Action indicates that Applicants did not attach a copy of the PTO Form 1449 to the Amendment filed August 12, 2002. As such, Applicants are attaching a copy of the Form PTO-1449. Each of the references listed on the Form PTO-1449 was cited in the Information Disclosure Sheet filed in the Patent Office on August 17, 2001. Copies of these references were also filed at that time. Therefore, the Information Disclosure Sheet was properly filed. The Examiner is requested to initial the Form PTO-1449 to show the consideration of each of the references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the above-identified application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-24 are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135

(Case No. 500.40501X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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Enclosures:

Version With Markings To Show Changes Made
PTO-1449 Form



Docket No. 500.40501X00

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 8-15 have been amended as follows:

1. (Twice Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit.

8. (Amended) The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal (VIN) is realized by a word line selecting signal; the driver circuit is realized by a word line driver; the first long-distance wiring is realized by a word line (WL); and the gate circuits are realized by memory cells.

9. (Amended) The semiconductor integrated circuit device as claimed in Claim 1, wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.

10. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the speed-increasing circuit includes an NMOS transistor and a buffer circuit is inserted at an input side of the second long-distance wiring.

11. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein the speed-increasing circuit includes a CMOS inverter having a PMOS transistor and an NMOS transistor.

12. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a plurality of speed-increasing circuits are additionally inserted between an intermediate position of the second long-distance wiring and the vicinity of the input terminal of the gate circuit connected to a position corresponding to the intermediate position.

13. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (VIN) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a plurality of buffer circuits are inserted at the input side of

the second long-distance wiring.

14. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (V_{IN}) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-increasing circuit, wherein a buffer circuit is inserted at the input side of the second long-distance wiring, and a buffer circuit is inserted at the output side of the second long-distance wiring.

15. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over an entire length of the first long-distance wiring, so that an input signal (V_{IN}) is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in a vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance wiring and a speed-

increasing circuit, wherein the input signal (VIN) is realized by a clock input signal (VCK); the driver circuit is realized by a clock driver; and the gate circuits are realized by flip-flop circuits.